IN THE CLAIMS

All currently pending claims and status indicators are set forth below:

1-13. (Canceled)

14. (Original) A method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, comprising the acts of:

receiving a first signal at a first input of a logical device, the first signal corresponding to a memory array block selection signal;

receiving a second signal at a second input of the logical device, the second signal corresponding to a testmode enable signal;

producing an output signal from the logical device, wherein the output signal corresponds to one of the first signal and the second signal;

enabling a plurality of memory array block select lines in response to the output signal from the logical device; and

writing data to a plurality of memory array blocks corresponding to the enabled memory array block select lines.

15. (Original) The method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, as set forth in claim 14, wherein the acts of receiving comprise receiving the first signal and the second signal at a NAND gate.

16. (Original) The method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, as set forth in claim 14, comprising:

producing an output signal from the logical device, wherein the output signal corresponds to the testmode enable signal;

enabling a plurality of memory array block select lines in response to the output signal, each of the plurality of memory array block select lines corresponding to one of a plurality of memory array blocks; and

writing data to the plurality of memory array blocks.

17-21. (Canceled)

22. (Previously presented) A method of programming/burning-in on SRAM comprises:

selecting a plurality of memory array blocks in the SRAM; and

simultaneously writing to each of the plurality of memory array blocks during burn-in testing.

23. (Previously presented) The method, as set forth in claim 22, wherein selecting comprises:

providing a block selection signal and a testmode signal to a logical device.

24. (Previously presented) The method, as set forth in claim 22, wherein selecting comprises:

providing a clock selection signal and a testmode signal to a NAND gate.

25. (Previously presented) The method, as set forth in claim 22, wherein simultaneously writing comprises transmitting data to a plurality of local write drivers.

26. (Previously presented) The method, as set forth in claim 25, comprising driving the data from each of the plurality of local write drivers to a respective one of the plurality of memory array blocks.

27. (Previously presented) A method of programming/burning-in an SRAM:

combining a plurality of signals produced externally with respect to the SRAM;

producing an internal signal configured to simultaneously select a plurality of memory array blocks in the SRAM; and

simultaneously writing to each of the plurality of memory array blocks.

28. (Previously presented) The method, as set forth in claim 27, wherein combining comprises combining the plurality of signals through a logical device located internally with respect to the SRAM.

29. (Previously presented) The method, as set forth in claim 28, wherein producing comprises producing an internal signal from an output of the logical device.

30. (Previously presented) The method, as set forth in claim 27, wherein combining comprises combining the plurality of signals through a logical device located internally with respect to the NAND gate.

31. (Previously presented) The method, as set forth in claim 27, wherein simultaneously writing comprises simultaneously writing to each of the plurality of memory array blocks during burn-in.

32. (Previously presented) The method, as set forth in claim 27, wherein simultaneously writing comprises transmitting data to a plurality of local write drivers.

33. (Previously presented) The method, as set forth in claim 32, comprising driving the data from each of the plurality of local write drivers to a respective one of the plurality of memory array blocks.